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All-optical NOR and NAND gates based on photonic crystal ring resonator

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ABSTRACT

We report a new configuration of all-optical logic gates based on two-dimensional (2D) square lattice photonic crystals (PCs) composed of silicon (Si) rods in Silica (SiO₂). The proposed device is composed of cross-shaped waveguide and two photonic crystal ring resonators (PCRRs) without nonlinear materials and optical amplifiers. The gate has been simulated and analyzed by finite difference time domain (FDTD) and plane wave expansion (PWE) methods. The simulation results show that the proposed all-optical logic gates could really function as NOR and NAND logic gates. This new device can potentially be used in large-scale optical integration and on-chip photonic logic integrated circuits.

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1. Introduction

All-optical signal processing techniques have attracted much attention due to their potential application in the field of optical communication and have been expected to be the main supporting techniques in future all-optical information networks [1,2]. As key components in all-optical networks, all-optical logic gates would achieve various networking functions [3,4] such as addressing, optical computing, clock recovery, header recognition, and signal regeneration, etc. Work reported to date, various technologies and materials have been introduced to realize all-optical logic gates including waveguide interferometers, optical fibers [5], semiconductor optical amplifiers [6–11] and photonic crystals [12–15].

But most of these works suffer from certain limitations such as big size, low speed and difficult to perform chip-scale integration. Generally, fiber-based logic gates are difficult to provide chip-scale integration. Semiconductor optical amplifiers are limited by their inevitable spontaneous emission noise. In order to design the logic gate with simple structure, ultra compact size, low power loss and high speed, we choose PCs. PCs have great advantages in designing ultra-compact all-optical integrated circuits with significant reduction in the size and power consumption. A lot of research works have been done in the field to realize and optimize the PCs

logic gates. Some of them are based on nonlinear optical effect [16–18], self-collimation effect [19,20], multi-mode interference [21], photonic crystal ring resonators [22–26] and Y-shaped PCs waveguide [27]. To our best knowledge, no optical logic gates have been proposed based on cross-shaped PCs waveguide combined with ring resonators.

In this paper, we have proposed a new symmetrical configuration of NOR and NAND all-optical logic gate based on cross-shaped PCs waveguide and two PCRRs composed of cylindrical silicon rods in SiO₂. This structure has the potentiality to be applied in photonic integrated circuits. The electromagnetic wave propagation in the time domain of the logic gate was simulated using two-dimensional FDTD, and photonic band gap has been calculated using PWE.

2. Device structure and operational principle

The schematic of proposed all-optical logic gate is shown in Fig. 1, consisting of two ring resonators embedded between three mutual vertical line defects. The inradius of the ring resonator is $R_{irr}=3a$, the exradius of the ring resonator is $R_{orr}=5a$, where “ a ” is the lattice constant. The length of two horizontal-waveguides is $L=13a$. The logic gate contains two input signals, a probe signal and an output signal. The left and right ports are indicated as input port A and input port B. The up port C is the probe signal, and the bottom port D is used to record the output intensity of the logic

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gate. We keep probe signal always “on” together with various combinations of input signal A and B , that is, “on” and “off”.

Two vertical-waveguides beside the bus-waveguide are introduced, as an important part in our logic gate. Due to the coupling effect, the light in two vertical-waveguides can couple to bus-waveguide and generate destructive interference with probe signal. Therefore the intensity of output can change with different state of the input signal.

If three or more rows of silicon rods are between bus-waveguide and two vertical-waveguides, the coupling effect is too weak and the proposed logic gate cannot work as we hoped. If only one row of silicon rods is between bus-waveguide and two vertical-waveguides, most of light in the bus-waveguide will couple to two vertical-waveguides therefore the output intensity is very low. To achieve the best coupling effect, two rows of silicon rods between bus-waveguide and two vertical-waveguides are selected, and the length of two vertical-waveguides is defined as H .

The proposed device is designed with square lattice PCs composed of $37a \times 27a$ 2D cylindrical silicon rods in SiO_2 with refractive index $n_{\text{Si}}=3.5$ and $n_{\text{SiO}_2}=1.45$. The dispersion diagram of this lattice, derived by the PWE method, is shown in Fig. 2. It demonstrates that this lattice has only a TE band gap. Therefore, the device has been designed for TE modes, with the magnetic field perpendicular to the rods. A shared broadband single-mode frequency exists that ranges from $0.270 (a/\lambda)$ to $0.321 (a/\lambda)$. For the 1550 nm communication window, the lattice constant of the PCs is selected to be $a=465$ nm. With comparison and simulation, $0.2a$ is the best size of Si rods radius for light to propagate in our proposed logic gate. Therefore the radius of the Si rods is selected

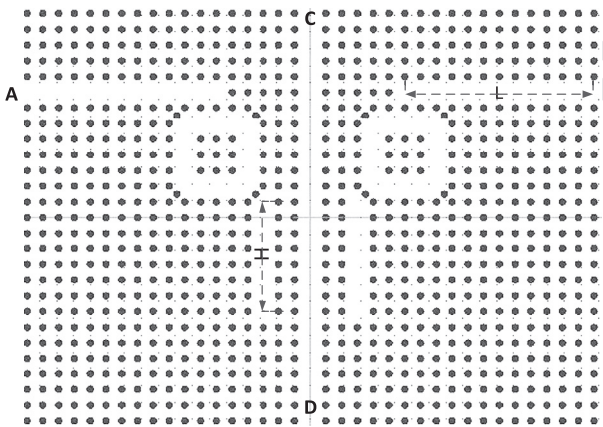


Fig. 1. Schematic structure of proposed all-optical logic gate.

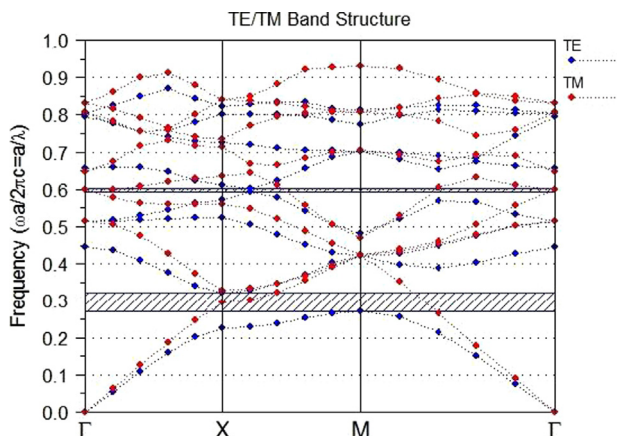


Fig. 2. Band diagram in a square lattice of Si rods in the SiO_2 substrate for TE and TM modes.

to be $r=0.2a$ to increase the transmissibility of the proposed structure.

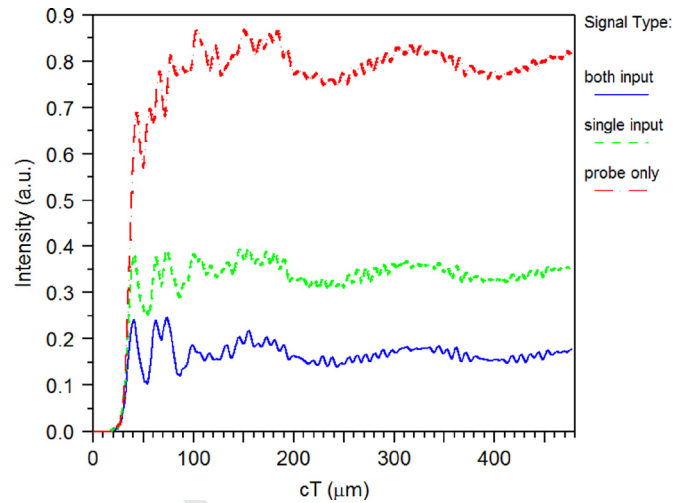


Fig. 3. Behavior of the proposed NOR gate.

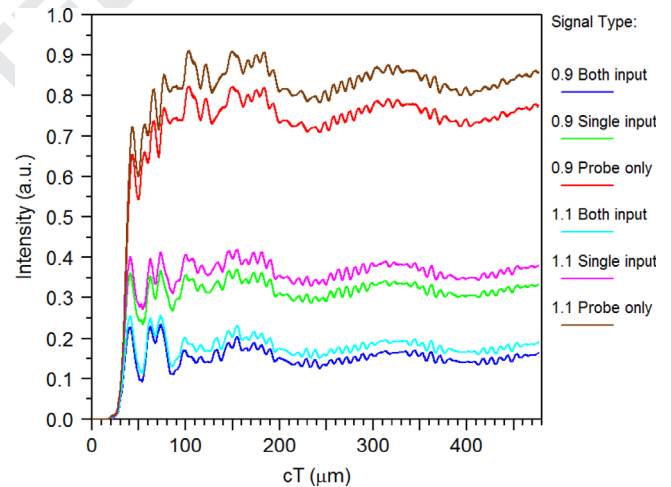


Fig. 4. Behavior of the different intensities of probe signal.

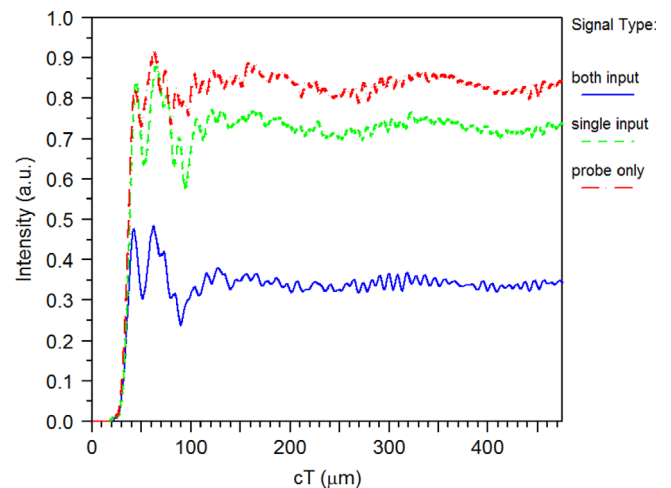


Fig. 5. Behavior of the proposed NOR gate.

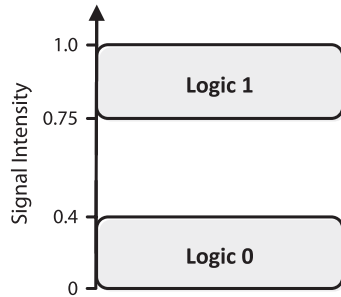


Fig. 6. Definition of "one" and "zero" logic levels.

Table 1

Truth table for our proposed NOR and NAND gates.

Input A	Input B	Probe	NOR	NAND
0	0	1	1	1
1	0	1	0	1
0	1	1	0	1
1	1	1	0	0

3. Simulation results and discussion

The two-dimensional FDTD method has been used to numerically analyze the light propagation behaviors in the proposed device. A wavelength $\lambda=1550$ nm, length of two vertical-waveguides and horizontal-waveguides are 8 and 13, i.e., $H_1=8a$ and $L=13a$, respectively, and the optical communication windows are used to show NAND and NOR logic gates operations of the device.

The intensity of input signal and probe signal are defined as P_0 to easier future explanation and calculation, and the probe signal is always launched from port C. If incident light is launched from two input ports, some portion of light will be coupled into bus-waveguide as mentioned above. Due to beam interference the intensity of output port D is different for different states of input port A and input port B, the result of simulation is shown in Fig. 3. As shown in Fig. 3, if no incident light is launched from two input ports A and B, the output intensity is greater than 75% and can reach 87%. If incident light is only launched from single input port A or B, the output intensity is less than 40%. And if incident light is launched from two input ports A and B concurrently, the output intensity is less than 25%.

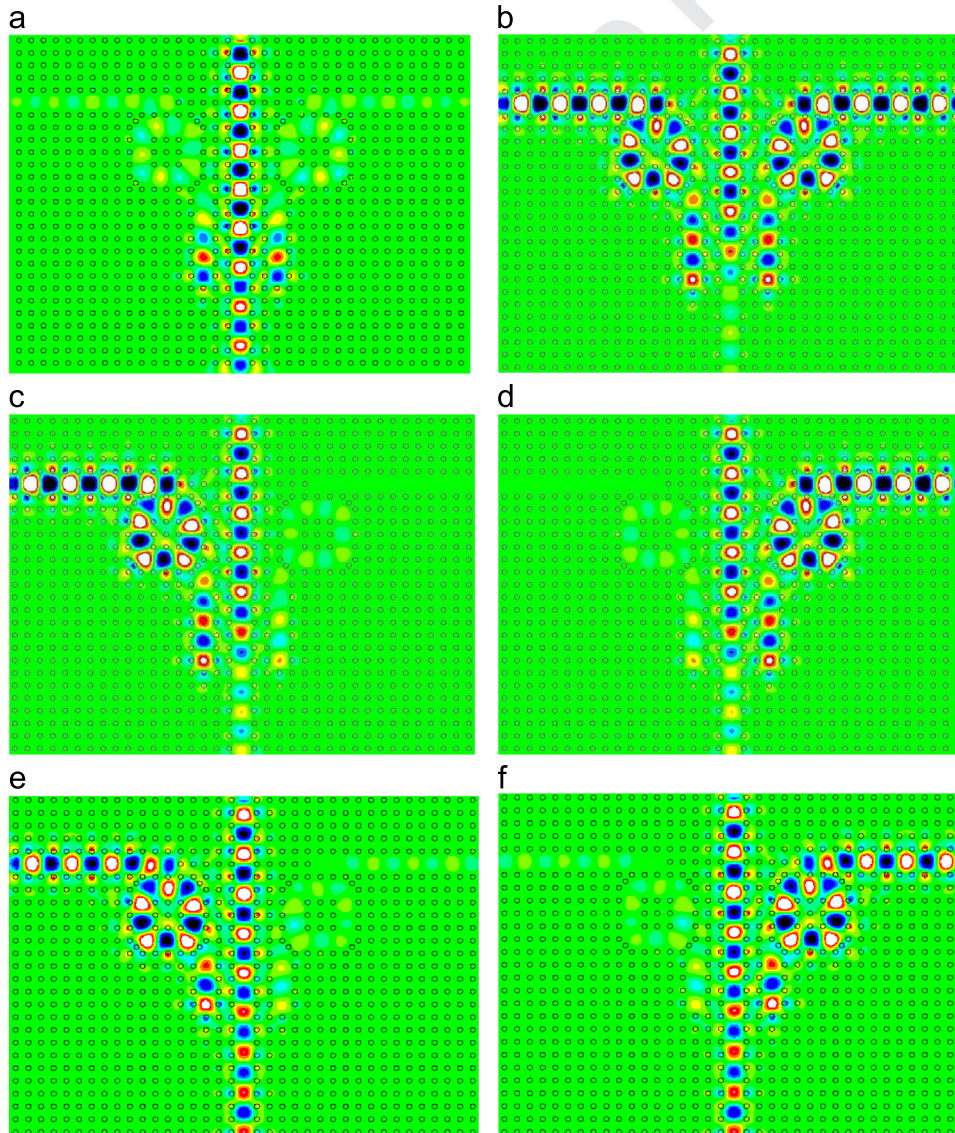


Fig. 7. Field distribution to show the performance of the proposed all-optical NOR gate. (a) $A=0, B=0$, (b) $A=1, B=1$, (c) $H=8a, A=1, B=0$, (d) $H=8a, A=0, B=1$, (e) $H=5a, A=1, B=0$ and (f) $H=5a, A=0, B=1$.

In consideration of the real intensity of probe signal may exceed or under P_0 , the intensity of probe signal has been changed to test the stability of the proposed logic gate, and the result of simulation is shown in Fig. 4. As the intensity of probe signal increased to $1.1P_0$, if no incident light is launched from input ports, the output intensity is greater than 80% and can reach 90%. If incident light is only launched from single input port, the output intensity is less than 42%. And if incident light is launched from two input ports A and B concurrently, the output intensity is less than 26%. As the intensity of probe signal decreased to $0.9P_0$, if no incident light is launched from input ports, the output intensity can reach 80%. If incident light is only launched from single input port, the output intensity is less than 38%. And if incident light is launched from two input ports A and B concurrently, the output intensity is less than 23%. So the stability of the proposed logic gate is well.

The intensity of output of all states will be changed for the length of two vertical-waveguides has changed. If the length of two vertical-waveguides is decreased to $5a$, i.e., $H_2=5a$ and the result of simulation is shown in Fig. 5. As shown in Fig. 5, if no incident light is launched from two input ports A and B, the output intensity is greater than 80% and can reach 90%. If incident light is only launched from single input port A or B, the output intensity is greater than 75%. And if incident light is launched from two input ports A and B concurrently, the output intensity is less than 40%.

According to the simulation results we mentioned above, logic 0 and logic 1 can be defined as larger than 75% and less than 40% respectively as shown in Fig. 6. The proposed logic gates have been simulated according to various possible combination of inputs (0, 0), (0, 1), (1, 0) and (1, 1), and the truth table for our proposed logic gates can be summarized in Table 1.

The behavior of proposed logic gates are shown in Fig. 7, where the incident light is continuous wave with 1550 nm wavelength, the L , H_1 and H_2 are $12a$, $8a$ and $5a$, respectively. As shown in Fig. 7, when the length of two vertical-waveguide is $8a$, i.e., $H=8a$, the proposed device can realize the function of NAND logic gate. When the length of two vertical-waveguide is decreased to $5a$, i.e., $H=5a$, the proposed device can realize the function of NOR logic gate. The simulation results further proved that this new configuration can really function as NOR and NAND gates.

4. Conclusions

In this paper, a new design of cross-shaped all-optical logic gate has been proposed in two-dimensional square latticed silicon rods in SiO_2 . The device performance was analyzed and simulated

by PWE and FDTD methods. By combining the functions of cross-shaped waveguide and two PCRRs, new ultra-compact photonic crystal logic NOR and NAND gates have been demonstrated. The definitions of logic 1 and 0 were also introduced. The dimension of the logic gate is not more than $6.8 \mu\text{m}$. Compared with nonlinear material logic gate, the proposed logic gate which is based on linear characteristics of the material can operate at low powers. It is expected that these new structures will make PCRRs have new applications for all-optical logic circuits and ultra-compact high density photonic integration.

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