

# Optimization of Insulator-Based Dielectrophoretic Devices

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## Abstract

Insulator-based dielectrophoresis (iDEP) employs arrays of electrically insulator posts in a microfluidic device to create dielectrophoretic forces that affect particle movement (Figure 1). The trapping performance of iDEP devices involves a careful balance between electrokinetics (EK) and dielectrophoresis (DEP), where EK is the superposition of electroosmosis (EO) and electrophoresis (EP). The design of the insulator posts is crucial for their dielectrophoretic performance. However, the a priori selection of an optimal design is challenging, given the large combinatorial of geometrical parameters (e.g., shape, length and width) and arrangement (e.g., lateral and longitudinal spacing) of the insulator posts [1].

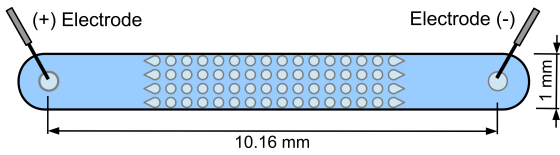
A parametric variation study was conducted to elucidate the set of design parameters that improve the trapping capacity of iDEP devices. The Laplace equation was solved using the AC/DC Module of COMSOL Multiphysics® software to estimate the distribution of the electric field, as well as the particle net force and velocity, within the array of insulator posts.

The parametric variation was used to design pseudo-optimal devices that enhance particle trapping and enrichment. The experimental trapping capacity of the pseudo-optimal designs is presented and discussed, showing a significant decrease in power consumption. The findings from this work provide a systematic approach towards the design of high performance iDEP devices for their lab-on-a-chip integration.

## Reference

[1] A LaLonde et al., Effect of insulating posts geometry on particle manipulation in insulator based dielectrophoretic devices, *Journal of Chromatography A*, 1344, 99–108(2014).

## Figures used in the abstract



**Figure 1:** Microchannel with electrically insulator posts.