SOI CMOS-based Transistor Model for Low Power Wireless Sensor Network

S. Panigrahi[1], P. K. Nanda[1]

[1]ITER, Siksha 'O' Anusandhan University, Bhubaneswar, Odisha, India

Abstract

Wireless sensor network has been extensively applied in a wide variety of areas such as defense, agriculture, transportation, etc. [1, 5]. The major challenge in those networks is the finite energy of the sensor node which is by and large engaged in transmitting and receiving data. It is known that substantial amount of energy is consumed in transmitter portion. The constituent unit of the transmitter i.e., LNA consumes the bulk of power [2, 3].
In this piece of work, we have addressed this issue with the use of SOI CMOS rather than the traditional CMOS [1]. It has been reported in the literature that SOI CMOS based circuits consumes low power and have low junction capacitance [1, 2, 5]. This in turn enhances the switching speed of the sensor node.
In this research, attempts have been made to reduce the internal capacitance and also the drain current which in turn reduce the power. The advantage of the SOI CMOS is that it has buried oxide layer above the silicon layer which helps in reducing the capacitance and also in drain current. In order to minimize the power consumption, the drain current needs to be minimized. In this regard we have proposed two SOI CMOS based topologies which are 1. Hole Model and 2. Sandwiched Model. In the Hole model, the oxide layer has been split into two parts leaving a hole in between layers where as in the Sandwiched model there are three oxide layers sandwiched above the substrate. Besides, there is a hole in between the oxide layers. Therefore this model can be viewed as three oxide layers with holes as shown in Figure 1.
The topologies of the above proposed models have been developed using COMSOL Multiphysics. The Bulk - Si CMOS model from the COMSOL library has been taken as the reference. All topologies have also been developed with available parameters in COMSOL Software.
The above three topologies have been simulated in the COMSOL and drain current with respect to the voltage was analyzed for each proposed model. Figure 2 shows the Vd-Ids characteristics for the Bulk - Si CMOS model. It has been observed that the drain current increases with increase in the drain voltage and the maximum drain current is 70mA while in the SOI CMOS it is 60mA as shown in Figure 3. The saturated drain current for our Sandwiched model is shown in Figure 4 and the drain current is observed to be 0.125mA. Thus there is a substantial reduction in drain current as compared to Bulk - Si CMOS.
The two proposed topologies exhibited reduced drain current and the reduction was found to be substantial as compared to Bulk -Si CMOS model. It has also been observed that the drain current is a function of the distance of separation between two oxide layers. For a certain distance of separation the drain current reduced substantially. Thus the two proposed models will be very

much useful while designing LNA for the sensor nodes.

Reference

[1] Takayasu Sakurai et.al, “Fully-DepletedSOI CMOS circuits and Technology for Ultra-low power Applications”, 2006, Springer
[2] Vivian Ma, “SOI vs CMOS FOR ANALOG CIRCUIT”, Technical Report, University of Toronto, 2001
[3] Y. Chen et.al, “An SOI-CMOS Low Noise Chopper Amplifier for High Temperature Applications”, Proceedings of IEEE on Integrated Circuits, pp 240 – 243, 2014
[4] M.T. Sanz et.al, “Self-cascode SOI versus Graded-channel SOI MOS Transistors”, Proceedings of IEEE on Circuits, Devices and Systems, vol 153, No 5, pp 461-465, 2006
[5] Brian Patrick Otis, Electrical Engineering and Computer Sciences, University of California, Berkeley, “Ultra-Low Power Wireless Technologies for Sensor Networks”, Phd Thesis, 2005

Figures used in the abstract

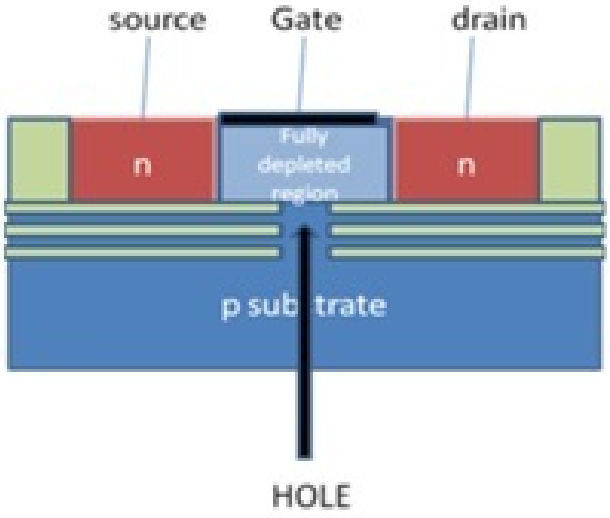

Figure 1: Figure -1.

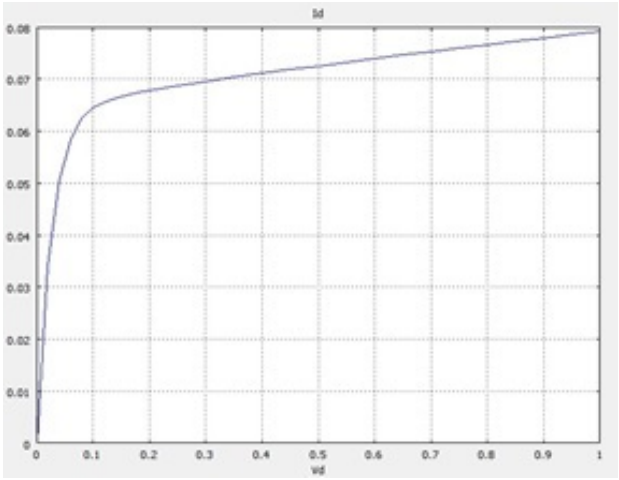

Figure 2: Figure - 2.

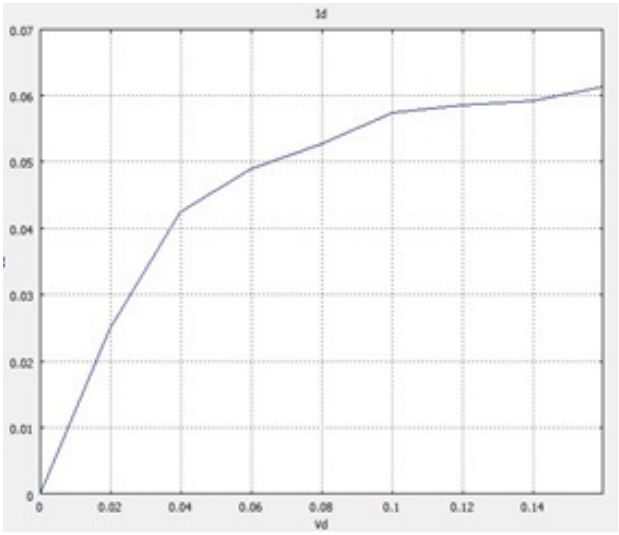

Figure 3: Figure - 3.

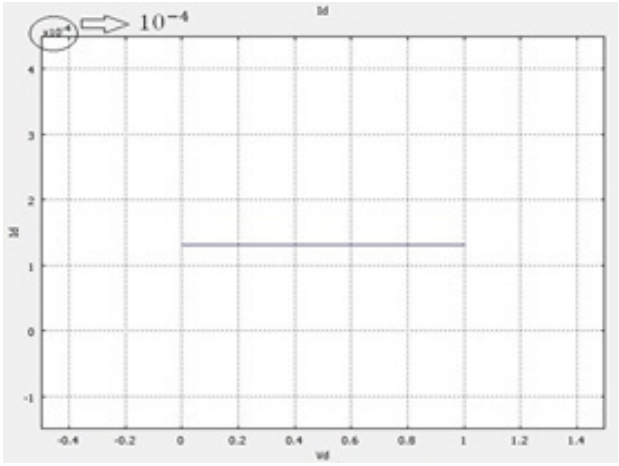

Figure 4: Figure - 4.