Numerical Thermo-Fluid Dynamics Modeling of a Processing Unit of the Fast Track Trigger for ATLAS

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Abstract: The aim of this work is the thermal modeling of a crate hosting boards with Associative Memories (AMs) designed for the Fast Tracker Trigger (FTK) system of the ATLAS detector at the CERN Large Hadron Collider (LHC). The crate is located in a rack where the cooling can be done with forced air, then the heat transfer is coupled to a non-isothermal fluid flow. Here COMSOL Multiphysics® has been used to investigate if a simplified geometry can give enough accurate results to well design the cooling system of the crate. This will enable the use of COMSOL also to well size the coolers of the rack.

Keywords: Conjugate heat transfer, Thermal management, Associative memories, FTK, Harsh environment.

1. Introduction

ATLAS is a general-purpose detector at the LHC [1]. It has been built for the detection of particles produced in proton-proton collisions at a center of mass energy of 14 TeV. The particles moving from the interaction point are detected by an inner tracking system (the Inner Detector in Fig. 1) surrounded by electromagnetic calorimeters, hadronic calorimeters, and the muon detectors.

The FTK is a highly paralleled hardware system designed to draw the global tracks of the particles moving in the inner detector. It uses the data from the 80 million of channels of the inner detector, identifying charged tracks and reconstructing their parameters at a rate of up to

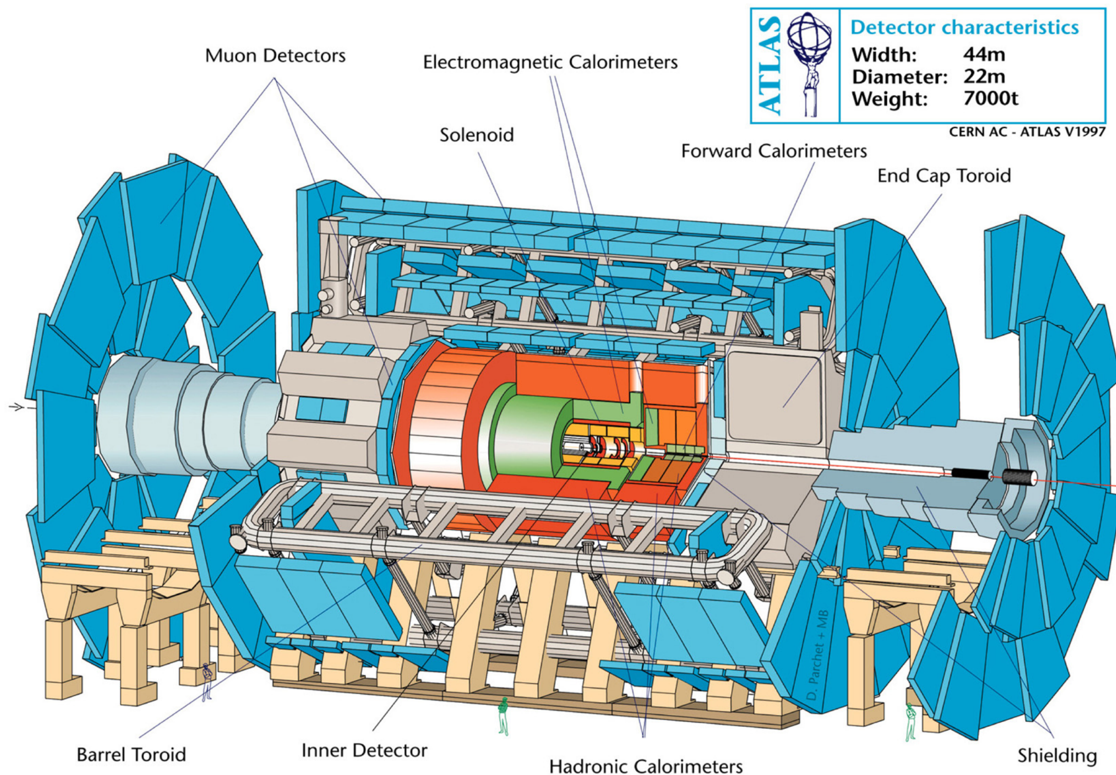

Figure 1. Cut-away view of the ATLAS detector [2].

100 kHz and within 100 μs. This performance is achieved by the FTK system utilizing the computing power of a custom Application-Specific Integrated Circuit (ASIC) with AMs designed to perform "pattern matching" at very high speed; track parameters are then calculated using modern Field Programmable Gate Arrays (FPGAs). The hardware system is based on AMs for pattern recognition and fast FPGAs for track reconstruction.

The Phase-2 upgrade of the LHC has been planned to be implemented in 2022, with a long shutdown. The detectors will be upgraded or substituted to improve the performances and sustain the higher rates and backgrounds at a new increased design luminosity. Also the trigger and data acquisition architecture will be upgraded to cope with the increasing rates.

The devices of the ATLAS experiment are located in a cavern 100 m underground, where the working conditions are severe. The great amount of memory needed by the FTK leads to a high density system. In these conditions, the cooling of the electronics with high power density is challenging [3, 4] and the design have to be made with the most advanced simulation techniques [5, 6].

Starting from a brief description of a rack where the AMs are placed, the following sections describe how the crate hosting AM boards can be modeled to simulate the heat removal and the results obtained.

2. The rack and the crate hosting the associative memories

In order to understand the boundary conditions to set in the model here presented, it can be useful to show how it is made the system where cases filled of AMs are embedded.

The AMs are hosted in a metallic crate suitable for a standard rack for electronic equipment. The rack hosts also the power supplies to feed the boards where are mounted the AMs. Power supplies and crates with AMs generate heat, which can be removed with a combined cooling system. To control the temperature inside the cavern where these electronic apparatuses are placed, a liquid cooling system capable to transmit the heat outside the cavern has to be used (and this also may be optimized by COMSOL, see for instance [7]). Then a rack with the layout shown in Fig. 2 has been made.

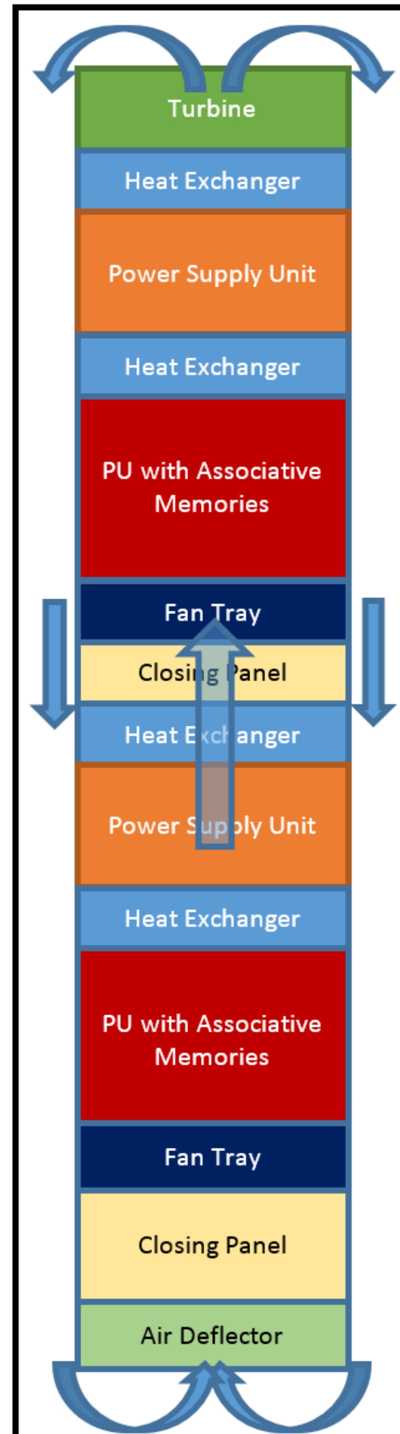

Figure 2. Schematic front view of the rack hosting the Processing Units with AMs.

The heat generated inside the rack is removed by mean of liquid heat exchangers (blue layers in Fig. 2), while the heat generated by the electronic devices inside the crates of the Processing Units (PU) and the power supply units is removed by the airflow (blue arrows in Fig. 2) generated by a turbine on the top of the electronic stack in the rack and trays with fans.

2.1 The crate

The crate where the AMs Boards (AMB) are located is shown in Fig. 3. It has 21 slots for boards and 6 holes matching the ones of the fan tray placed at the bottom when mounted in the rack. The top is open to allow the air flowing, while all around the case is closed by aluminum plates.

The PU crate is filled as shown in Fig. 4. One slot is taken by a controller of the AMBs. The others 20 slots are taken by a 4x repetitive sequence of four AMBs and a board with auxiliary and communication circuits.

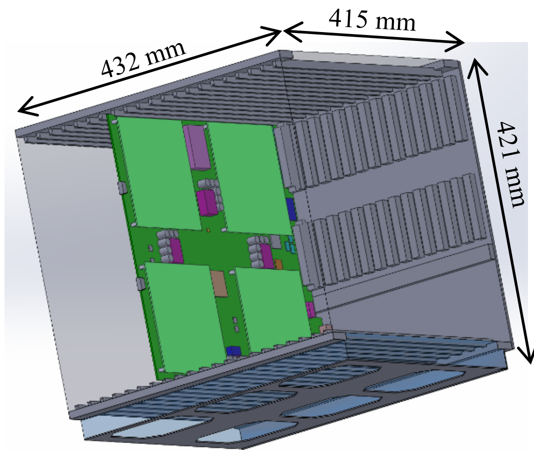

Figure 3. Sketch of the PU crate with one AMB.

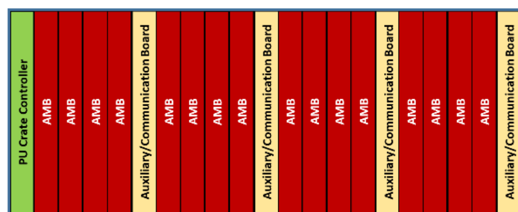

Figure 4. Layout of the boards mounted in the PU crate.

The heat generated in the controller and in an auxiliary/communication board is expected to be of the same order of magnitude, but less, than the one generated by an AMB.

As already stated, the AM system consists of AM chips, ASICs designed and optimized for this particular application, and two types of boards: the Local Associative Memory Board (LAMB), a mezzanine where the AM chips are mounted, and the AMB, which holds four LAMBs (Fig. 5). Both the AM chip and the two boards have a long development history and the power consumption, that takes place mainly in the AM chips, varies depending on the version of these chips. The estimated PU crate power consumption for the final system is more than 5 kW, which makes the design of the rack cooling system challenging.

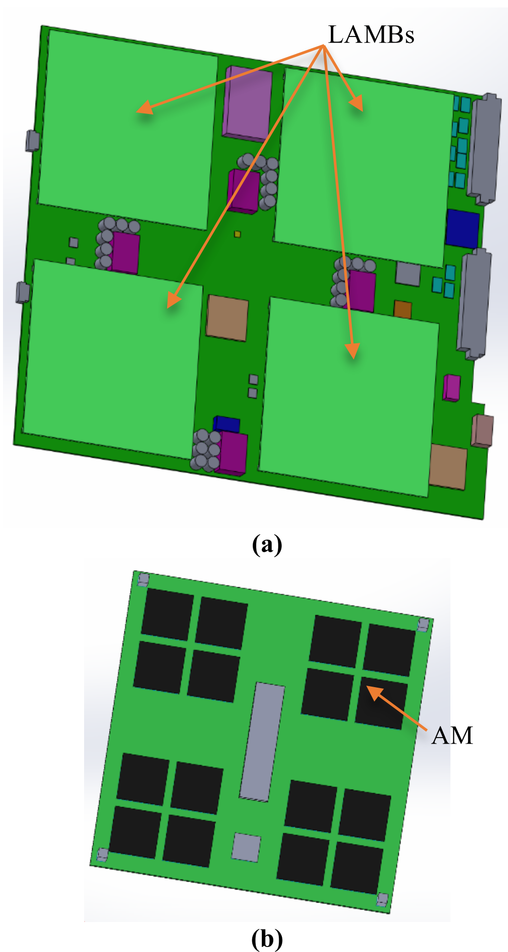

Figure 5. Layout of the board with AMs: (a) AMB; (b) AM side view of the LAMB.

3. Use of COMSOL Multiphysics® Software

Since the first trial of simulations it has been noticed that a detailed 3D geometry of the whole crate results in a FEM model with too high degrees of freedom, so it cannot be solved even by an advanced workstation. Thus, first of all, the 3D geometry of AMB and LAMB have been simplified, removing all the devices that are not thermally significant and that will not affect significantly the airflow (smaller parts). The radial capacitors (see grey cylinders in Fig. 5(a)) have been kept because the airflow is surely affected by them, but they were modeled in a simplified way, by hexahedral of the same sizes (height and diameter).

Moreover, to simplify the analysis, 1/3 of the whole PU crate has been drawn (Fig. 6), because the fans at the bottom inlets are placed as a 2 rows x 3 columns matrix, and preliminary isothermal CFD simulations have been shown an almost repetitive air flow respect to the 3 columns. Instead the layout of Fig. 4, has been considered the worst thermal case of the crate filled only by AMBs.

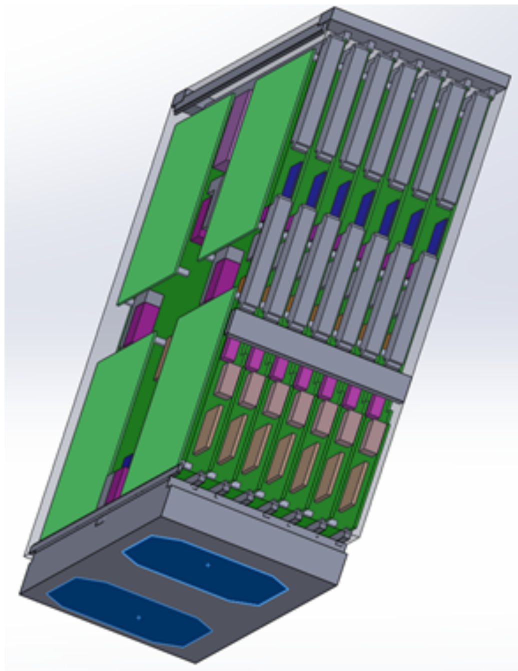

Figure 6. 3D geometry of the simplified 1/3 of the PU crate used for simulations.

COMSOL Multiphysics has been used to setup a numerical model of the Heat Transfer (HT) in solids and fluids problem coupled the Turbulent Flow of the air resulting from the fans (RANS – algebraic yPlus with compressible flow – Ma < 0.3).

3.1 Boundary conditions

The boundary conditions set at the surfaces of the inlet and the outlet of the crate are shown in Fig. 7.

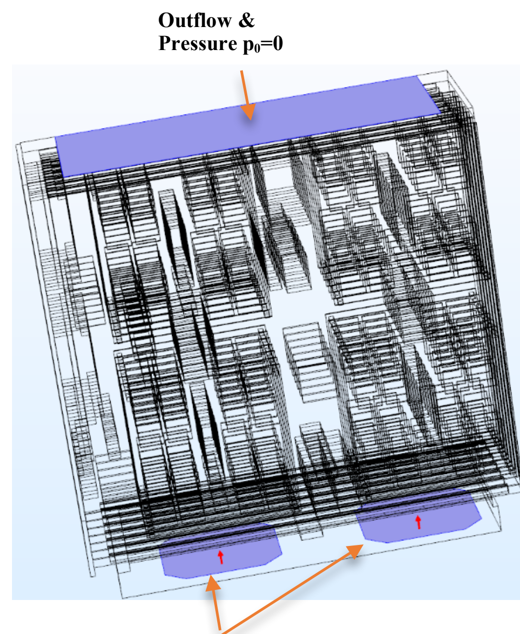

Figure 7. Conditions set at the boundaries of the inlet (bottom blue surfaces) and the outlet (top blue surfaces) of the reduced crate to simulate.

On all other external surfaces has been set a thermal insulation condition for the HT physic, while for the CFD problem has been set a no slip condition on all the wall in contact with the air.

3.2 Heat sources

The AMs volumes (Fig. 8), assumed made of ceramic material with a thermal conductivity of 15 W/(m·K), have been set as heat sources, each one with an overall heat transfer rate of 2.5 W (3x1120 W to remove from the whole PU crate).

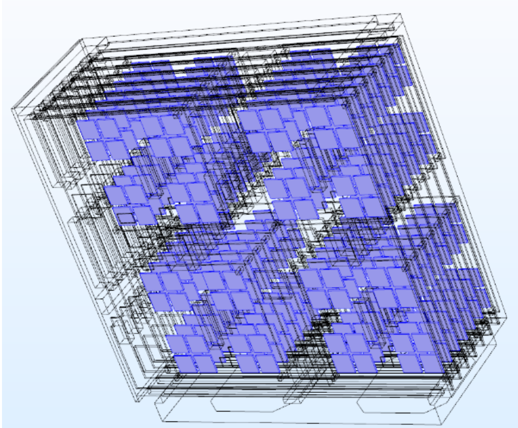

Figure 8. Volumes (highlighted blue) considered as heat sources.

8. Results

The results obtained by the stationary simulation with a dissipated power of 2.5 W per AM chip, and a temperature of the air at the fans of 20 °C, can be summarized by the air speed and the temperature maps in Figs. 9 and 10.

The air flows without high vorticity, once it enters between the boards.

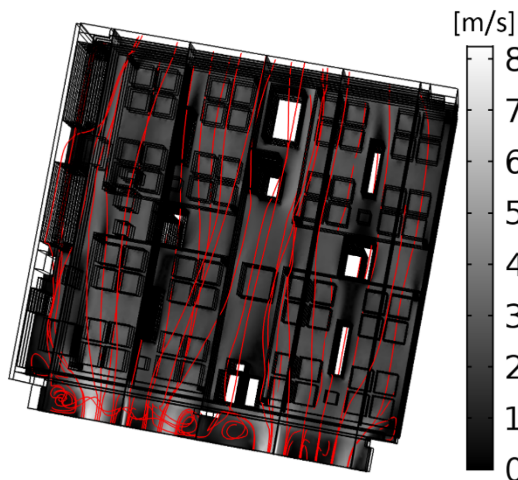

Figure 9. Air speed in a slice between the two AMB in the middle of the 1/3 simulated crate.

The AMB shown in Fig. 10 is the hottest, with T_{max}=72°C, because the slower air speed. Anyway, the maximum temperature of all the other AMBs is almost the same, few degree less than 72°C.

It has to be noticed that 70°C could be considered a safe value for the AM chips.

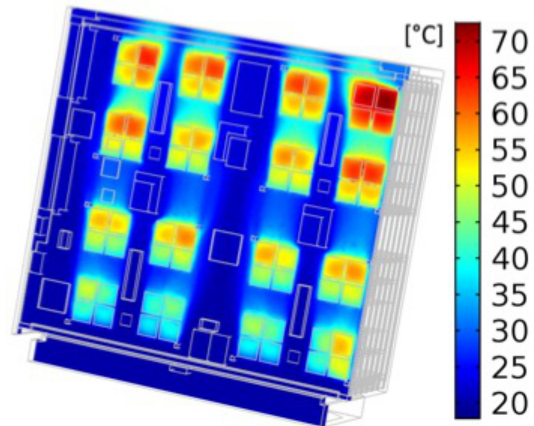

Figure 10. Thermal map of a slice passing through AM chips of the AMB close to the crate wall (hottest board).

8. Conclusions

The simulated thermal map matches quite good the preliminary measurement tests, thus this COMSOL model will be helpful for sizing the cooling system of future revisions of the presented system.

9. References

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