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Chip Drop after Silver Sintering Process

Dipl.- Phys. Kai Gruber

Fraunhofer Institute for
Silicon Technology

kai.gruber@isit.fraunhofer.de

Comsol Conference 2009
Milan, Italy

Fraunhofer
ISIT

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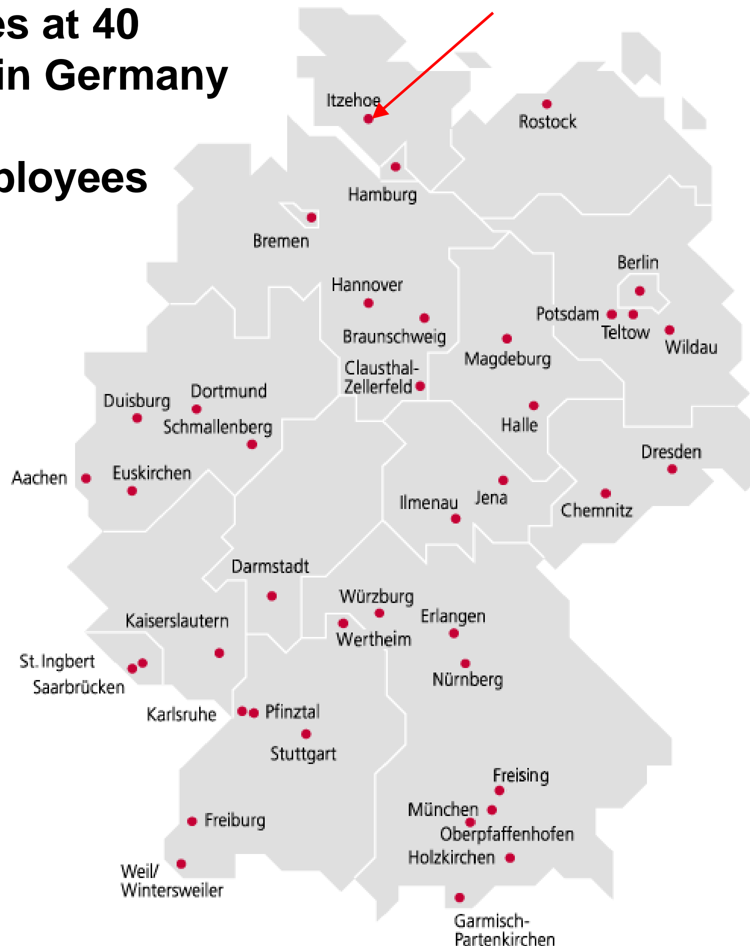
Fraunhofer Gesellschaft

57 Institutes at 40 Locations in Germany

15.000 Employees
1.4 B€/ a

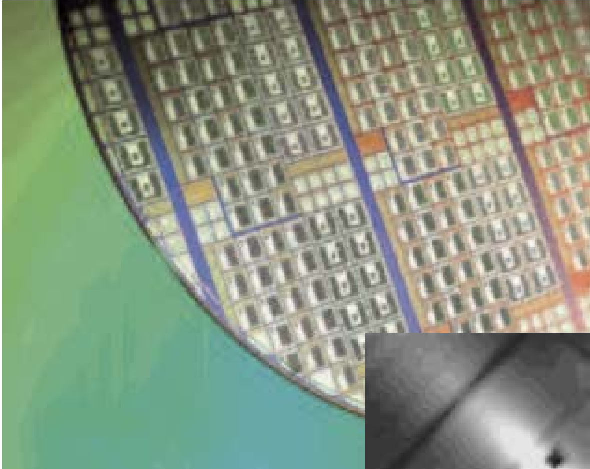


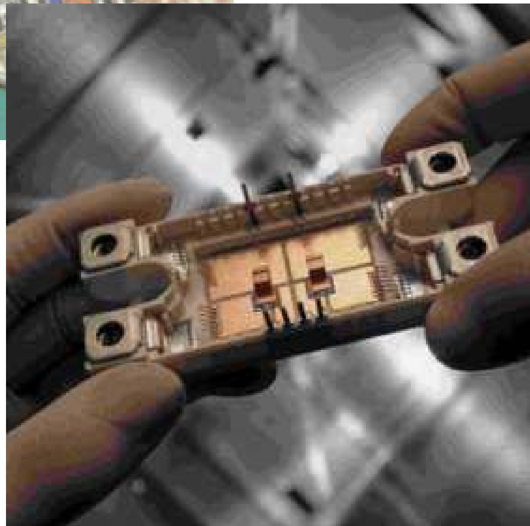
Research and Development-center for Microelectronics and Microsystems Technology

Certified: ISO 9001:2000

Research and Development for Power Devices

Areas of Competence in Power Electronics





- Discrete Power Devices

  (e.g. PowerMOS, IGBTs, Diodes)
- Simulation and Design
- Assembly, Power Modules
- Test and Reliability
- Failure Analysis and

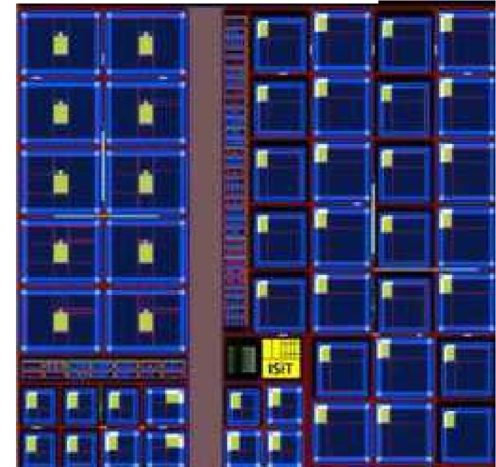
  Material Characterisation

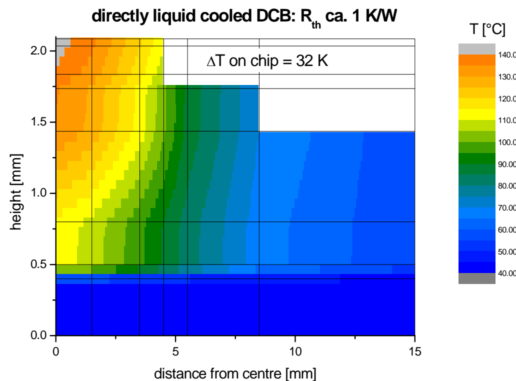
IC Technology and Power Electronics

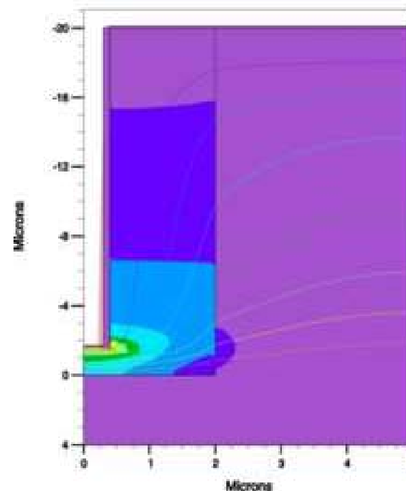
Design and Simulation for Power Devices

- Components Design with Cadence
- Thermal Simulation
- Components Simulation

IGBT Layout



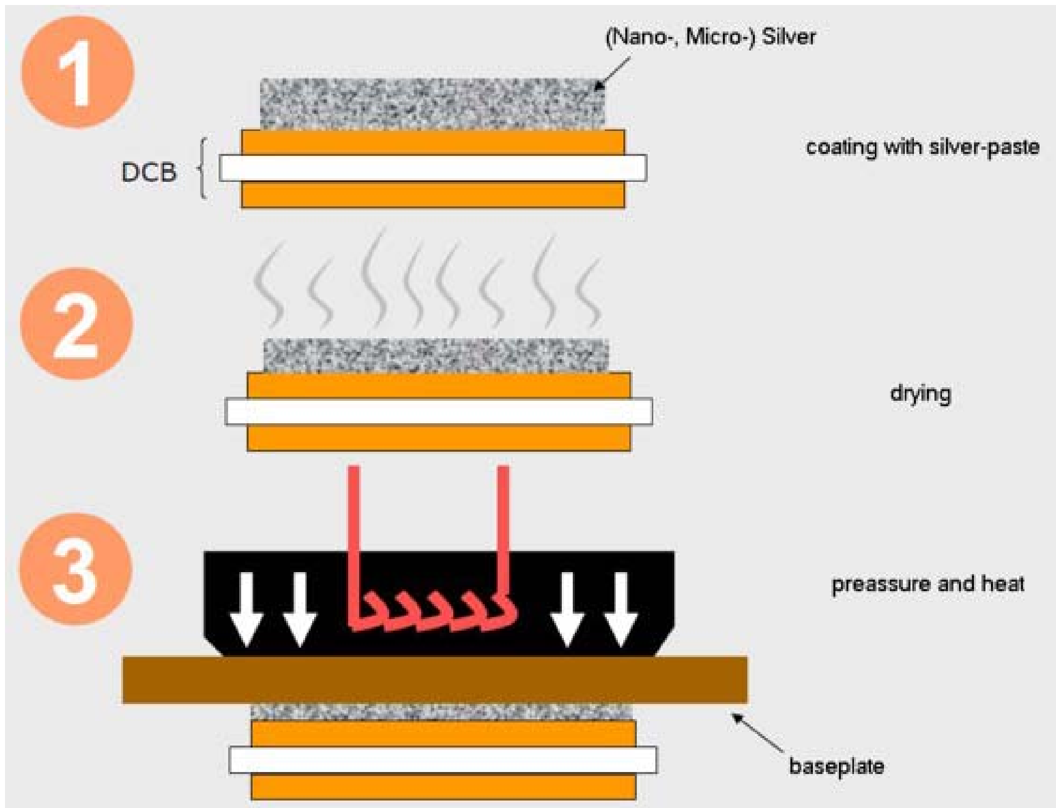


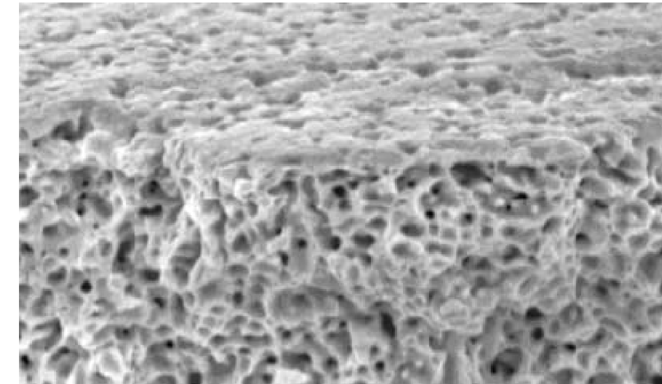


Simulation of a PowerMOS Device

outlook to future joining technologies

Silver Sintering Process

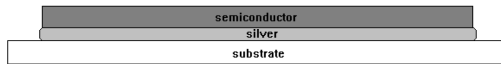


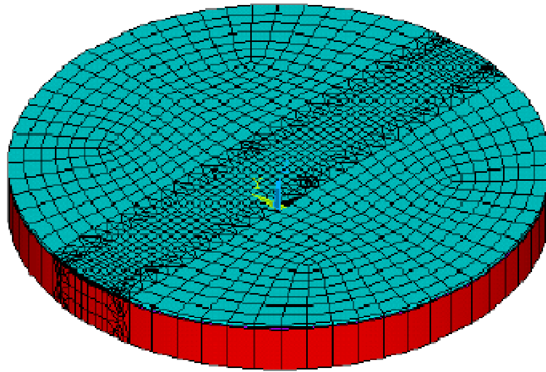

silver sintered layer (REM)

- excellent thermal and electrical conductivity
- melting point at 961°C
- high mechanical robustness

Source: Prof. R. Eisele, FH Kiel 2009

Problem

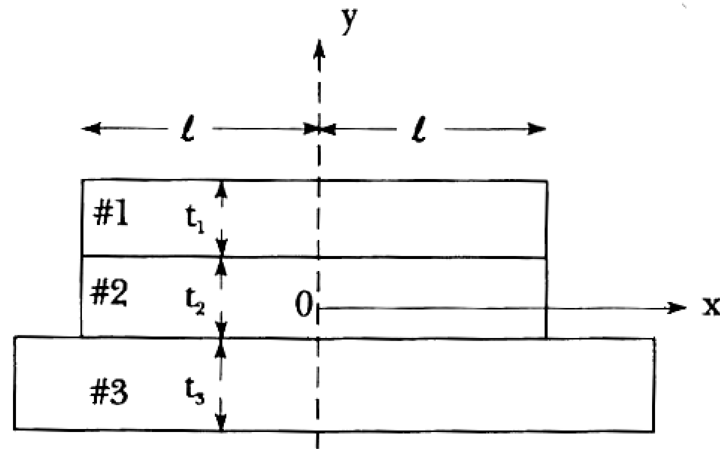


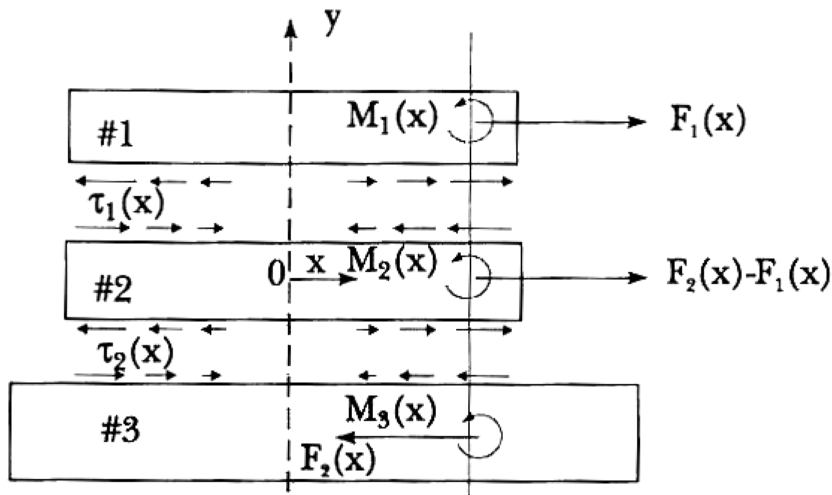


We used a stack with the following parameters:

- The 1st layer: pure copper, thickness of 800µm.
- The 2nd layer: pure silver, thickness of 30µm.
- The 3rd layer: pure silicon, thickness of 70µm
- temperature gap of 200 Kelvin
- radius of 4,5mm

Problem





Suhir´s Modell

$$\frac{1}{r(x)} = \frac{t\Delta\alpha\Delta T}{2\lambda D}\left(1 - \frac{\cosh kx}{\cosh kl}\right)$$

Normal stresses find her maximum at the interfaces and will be, on the bottom of the chip:

$$\sigma_{1b} = \frac{\Delta\alpha\Delta T}{\lambda t_1}\left(1 + 3\frac{tD_1}{t_1 D}\right)\left(1 - \frac{\cosh kx}{\cosh kl}\right)$$

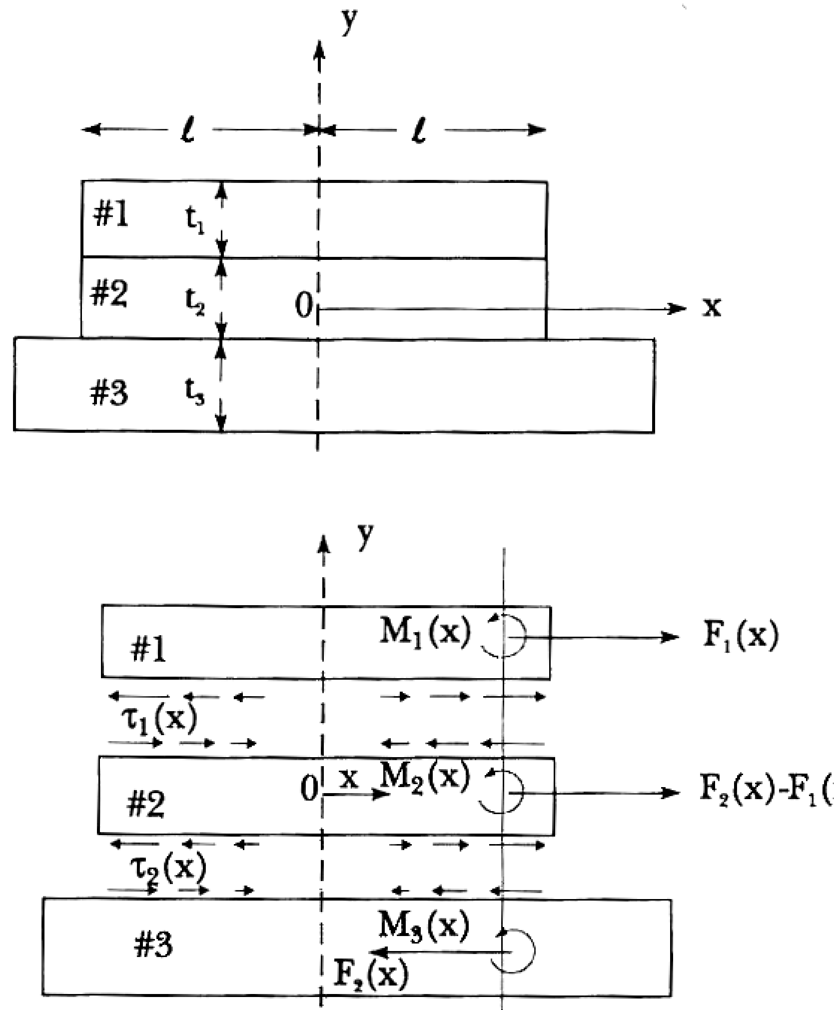
And on the top of the chip:

$$\sigma_{1t} = \frac{\Delta\alpha\Delta T}{\lambda t_1}\left(1 - 3\frac{tD_1}{t_1 D}\right)\left(1 - \frac{\cosh kx}{\cosh kl}\right)$$

The peeling stresses are due to forced bending of the stack despite differences in flexural rigidity of the components. The differences in adherent thickness and flexural rigidities $\mu = (t_3 D_1 - t_1 D_3)/2D$ lead to:

$$p(x) = -\frac{\mu}{\kappa}\Delta\alpha\Delta T\frac{\cosh kx}{\cosh kl}$$

Problem



Suhir´s Modell

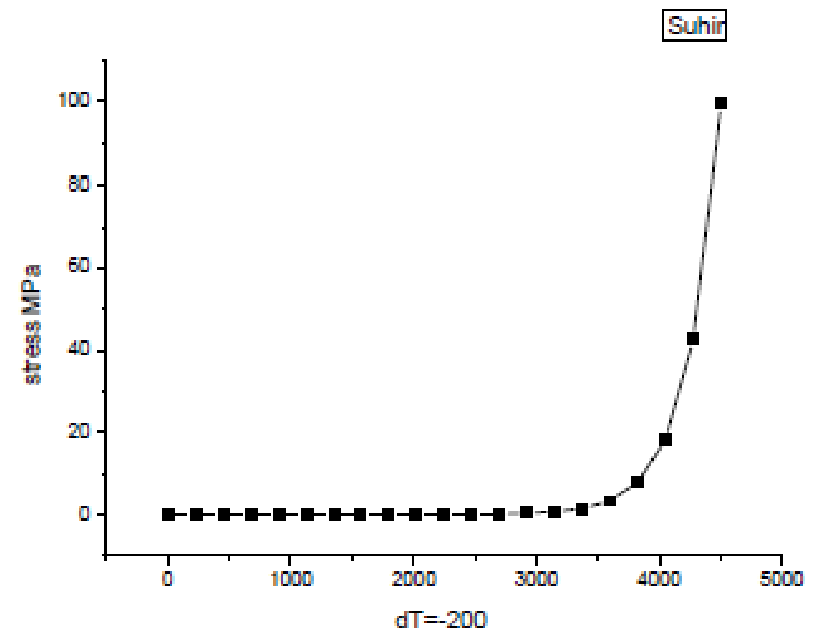


Figure 5: Numerical solution for S_{xz}, Suhir

2D-Axially-Symmetric or 3D

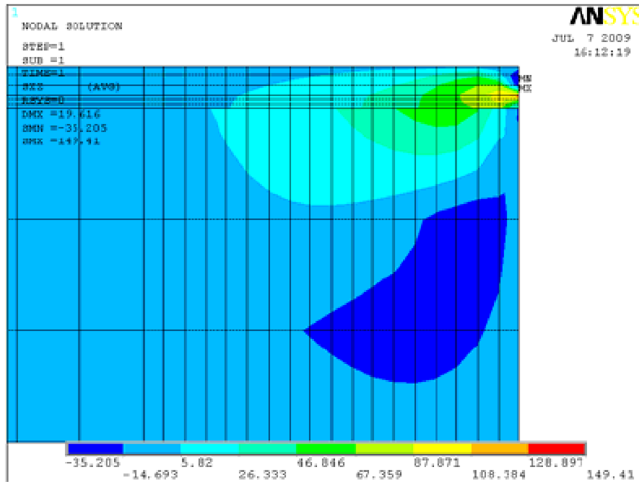


Figure 6: Shear stress, S_{xz}, 3D-model

We can not see great differences between the 3-dimentional and 2-dimentional axially symmetric model, even though we take a closer look over all stress components. We can see that the graphs of the different components almost lie on top

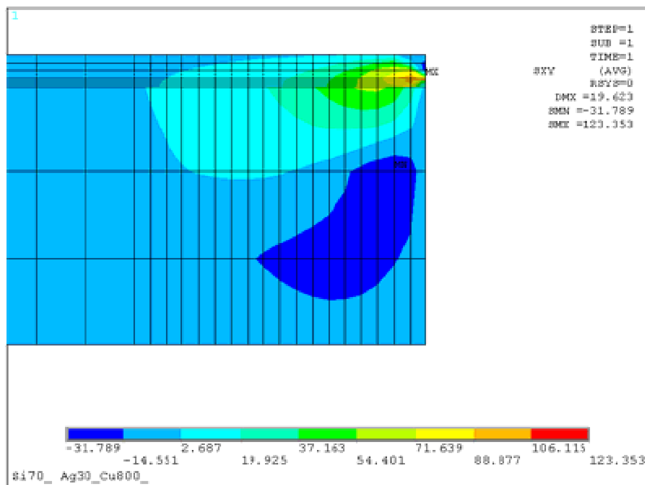


Figure 7: Shear stress, S_{xz}, 2D-axially symmetric

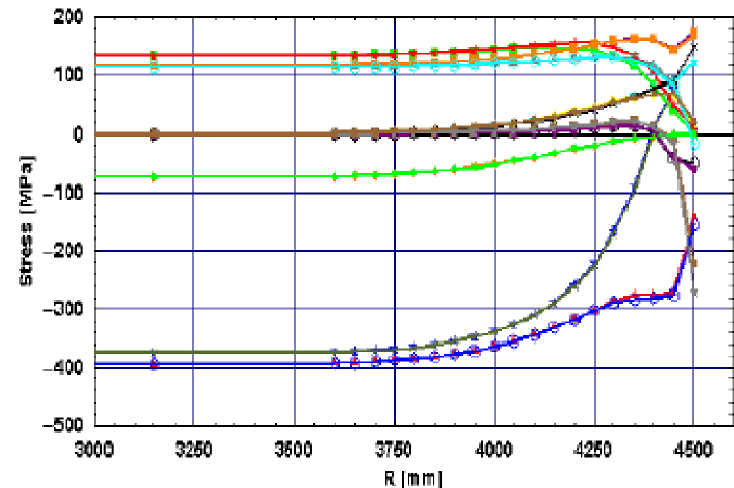
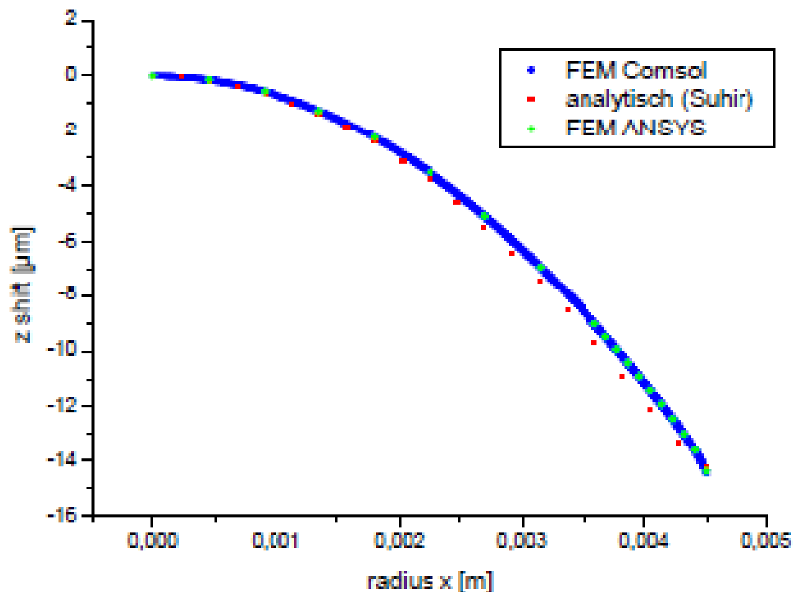


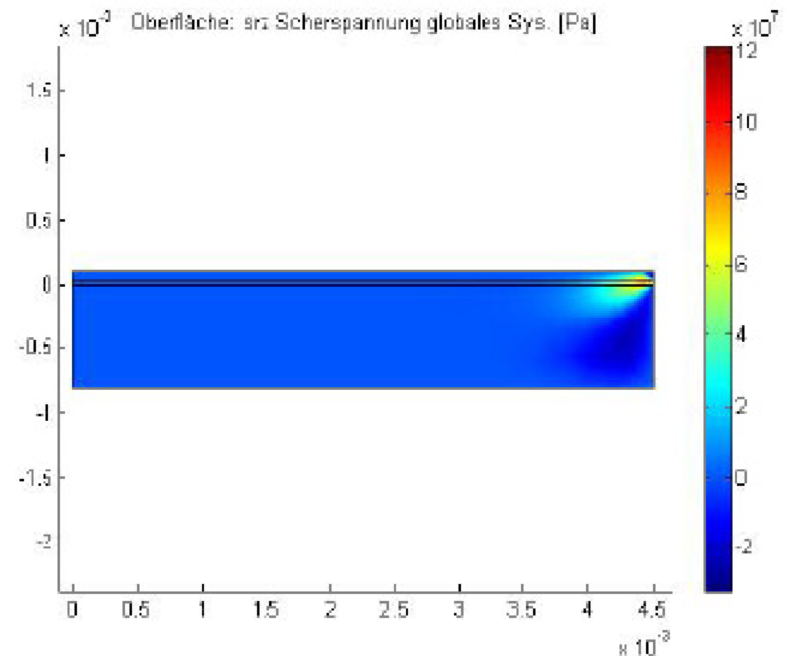
Figure 8: Stress, 3D and 2D-axially symmetric

COMSOL and ANSYS

We compare the z-displacement in both FEM-tools with Suhir´s model



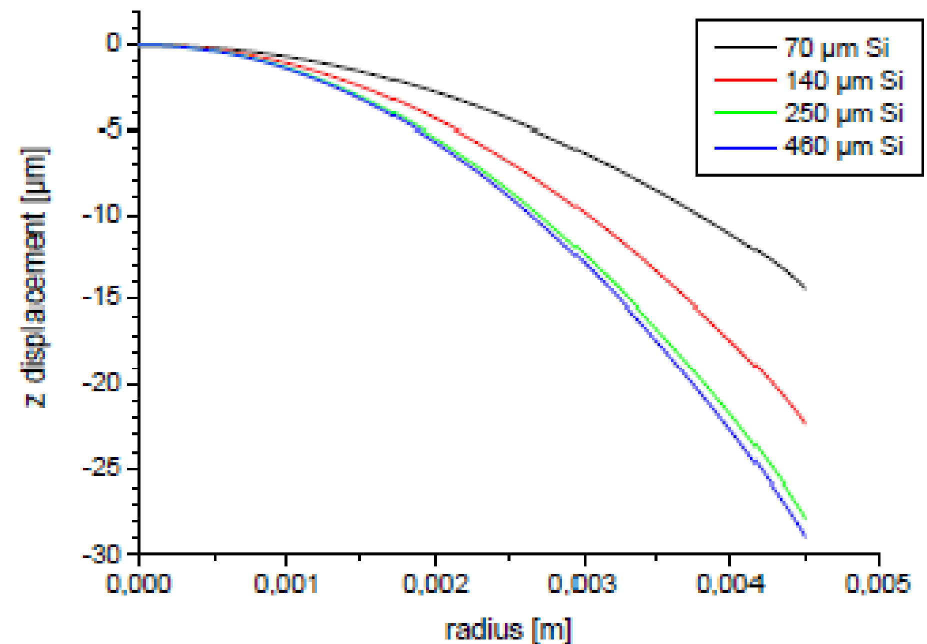
In both simulation tools we find a maximum



Chip Thickness

we have made a variation of the thickness of the chip with COMSOL and take a look at the z-displacement.

We solve variants of the thickness with 70, 140, 250 and 460µm.



Thank you very much for your attention!

Questions?

kai.gruber@isit.fraunhofer.de